Variable Block Adder (1D)

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https://en.wikipedia.org/wiki/AND_gate
https://en.wikipedia.org/wiki/OR_gate
https://en.wikipedia.org/wiki/XOR_gate
https://en.wikipedia.org/wiki/NAND_gate

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Variable size Block Carry Skip Adder (1)

The performance can be improved, ie.
all carries propagated quickly
by varying the block sizes

Accordingly the initial blocks of the adder are
made smaller so as to quickly detect carry generates
that must be propagated the furthers,

the middle blocks are made larger
because they are not the problem case,

and then the most significant blocks are again
made smaller so that the late arriving carry inputs
can be processed quickly

https::/electronics.stackexchange.com/questions/21251/critical-path-for-carry-skip-adder

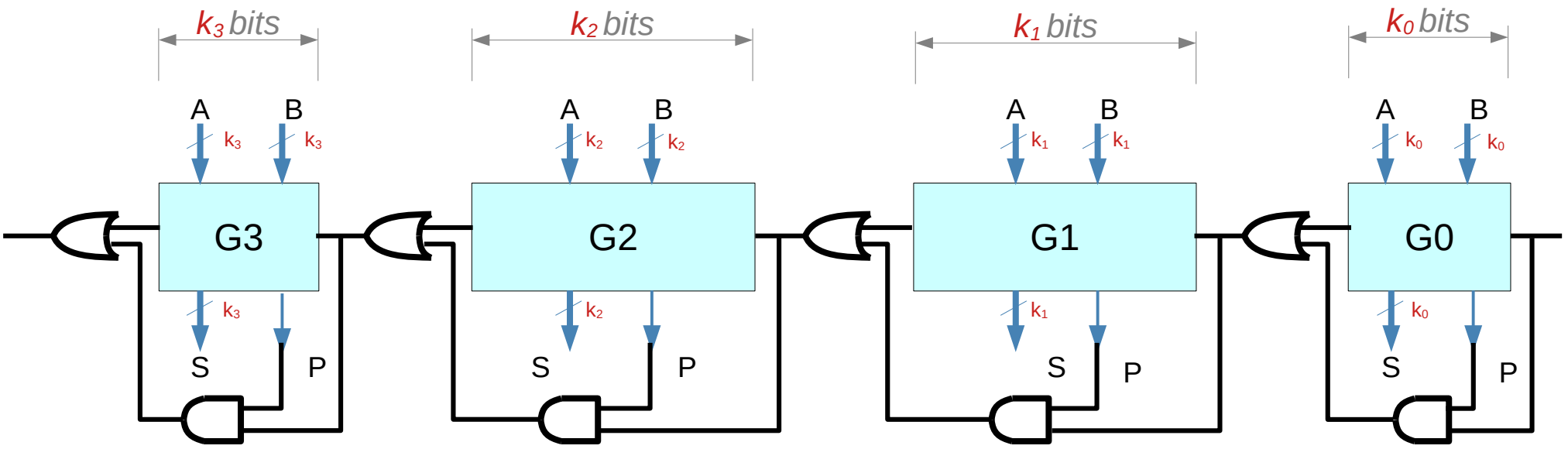
Variable size Block Carry Skip Adder (2)

In the next development there are R carry-skip blocks with sizes k_{R-1} , · · · , k_1 , k_0 ($n = k_{R-1} + \cdots + k_1 + k_0$) going from left to right.

Variable-size block CSA (VCSA)

R groups

$$n = \sum_{i=0}^{R-1} k_i$$



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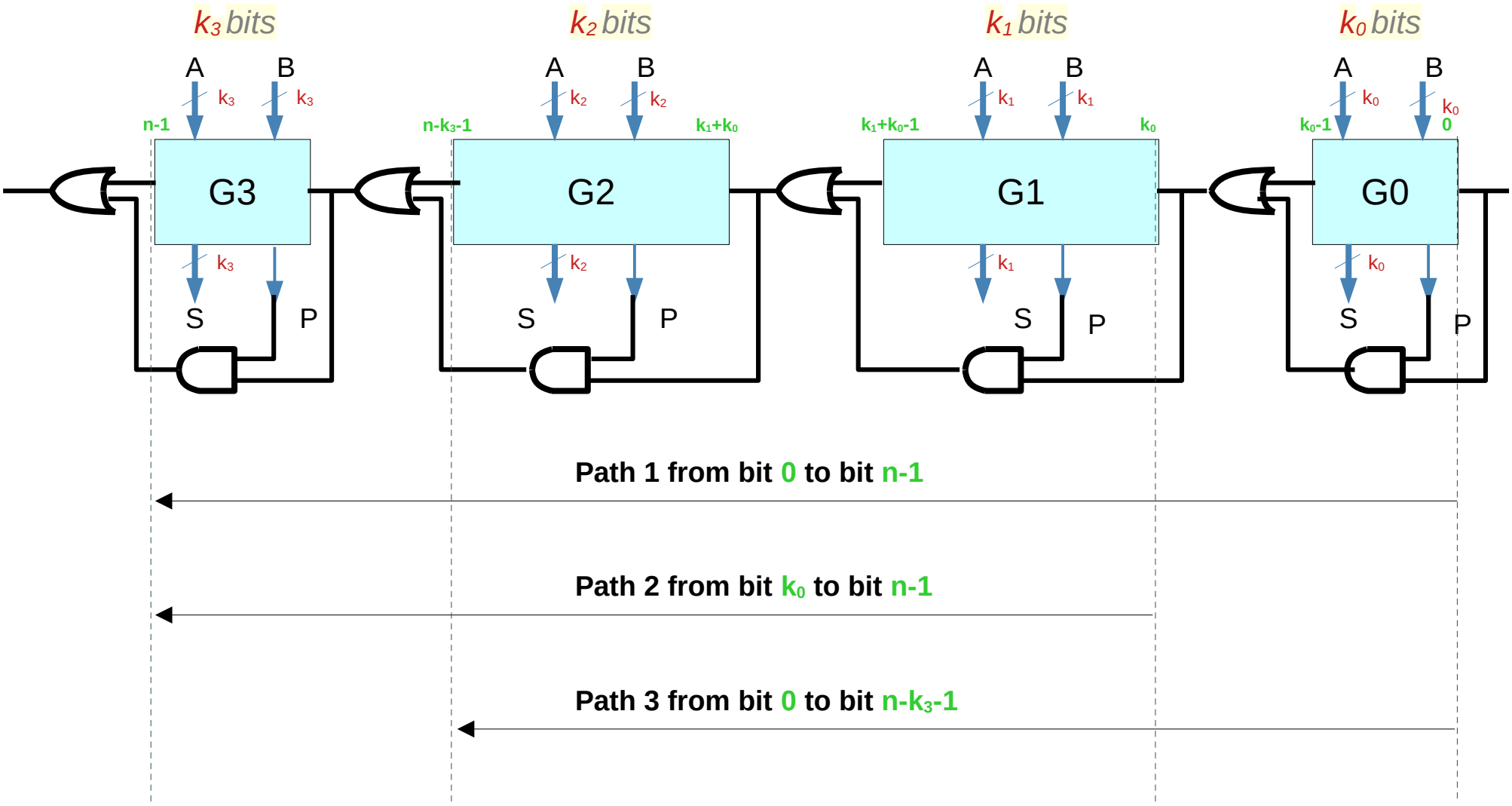
1. **k ← n : total number of bits**
2. **b ← k : block size in bits**

Variable size Block Carry Skip Adder (3)



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1. k ← n : total number of bits
2. b ← k : block size in bits

Variable size Block Carry Skip Adder (4)

Variable-size block CSA (VCSA)

Consider the equation for the worst case delay from stage 0 to stage n-1, corresponding to path 1

$T_{var-carry-skip} = T_{path\ 1}$

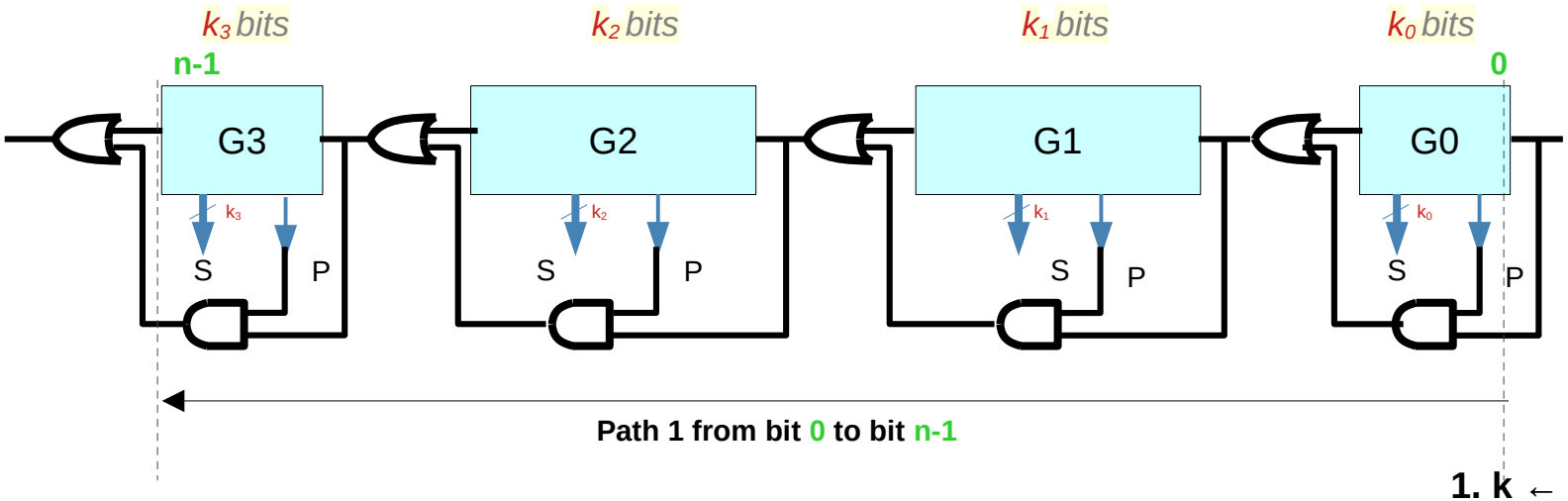
$= (k_{R-1} - 1)T_p + (R - 2)T_s + D + (k_0 - 1)T_p$

last block — middle blocks — OR — first block

$n = k_{R-1} + \cdots + k_1 + k_0$

R groups

$$n = \sum_{i=0}^{R-1} k_i$$



1. k ← n : total number of bits
2. b ← k : block size in bits

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Variable size Block Carry Skip Adder (5)

$T_{var-carry-skip} = T_{path\ 1}$

$= (k_{R-1} - 1)T_p + (R - 2)T_s + D + (k_0 - 1)T_p$

last block — middle blocks — OR — first block

- a carry being generated by stage 0 in block G0
  propagating through the (k_0 −1) remaining stages of block G0,
- then through the carry skip units of (R-2) blocks,
- then through (k_{R-1} − 1) stages of the left-most (last) block.

Variable-size block CSA (VCSA)

R groups

$$n = \sum_{i=0}^{R-1} k_i$$

1. k ← n : total number of bits
2. b ← k : block size in bits

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Variable size Block Carry Skip Adder (6)

Variable-size block CSA (VCSA)

Consider a carry being generated at the stage k_0,
the right-most stage of block 1,

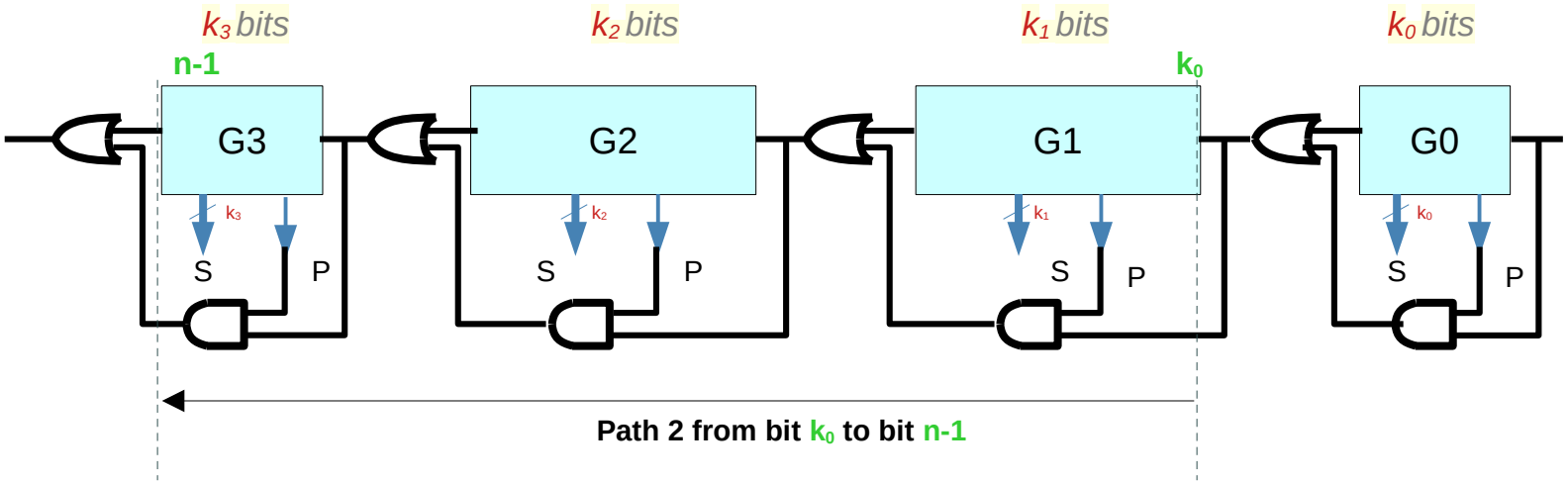
and following path 2 to the left-most stage n-1 of the adder.
It's delay would be:

R groups

$$n = \sum_{i=0}^{R-1} k_i$$

$$T_{path\ 2} = (k_{R-1} - 1)T_p + (R - 3)T_s + D + (k_1 - 1)T_p$$

last block middle blocks OR first block



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Variable size Block Carry Skip Adder (7)

Variable-size block CSA (VCSA)

R groups

$$n = \sum_{i=0}^{R-1} k_i$$

Path 1 has R blocks and R-2 middle blocks
Path 2 has R-1 blocks and R-3 middle blocks

$T_{path\ 1} = (k_{R-1} - 1)T_p + (R - 2)T_s + D + (k_0 - 1)T_p$
$T_{path\ 2} = (k_{R-1} - 1)T_p + (R - 3)T_s + D + (k_1 - 1)T_p$

$T_{path\ 1} = T_{path\ 2} \Rightarrow T_s + (k_0 - k_1)\,T_p = 0$
$T_s = T_p \Rightarrow 1 + (k_0 - k_1) = 0$

If $T_s = T_p$ then block G1 with the size of k_1 bits
can be 1 bit larger than block G0 with the size of k_0 bits
without making this delay path worse than path 1.

$T_s + (k_0 - k_1)\,T_p = (1 + (k_0 - k_1))T_p = 0$

$k_1 = k_0 + 1$

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1. k ← n : total number of bits
2. b ← k : block size in bits

Variable size Block Carry Skip Adder (8)

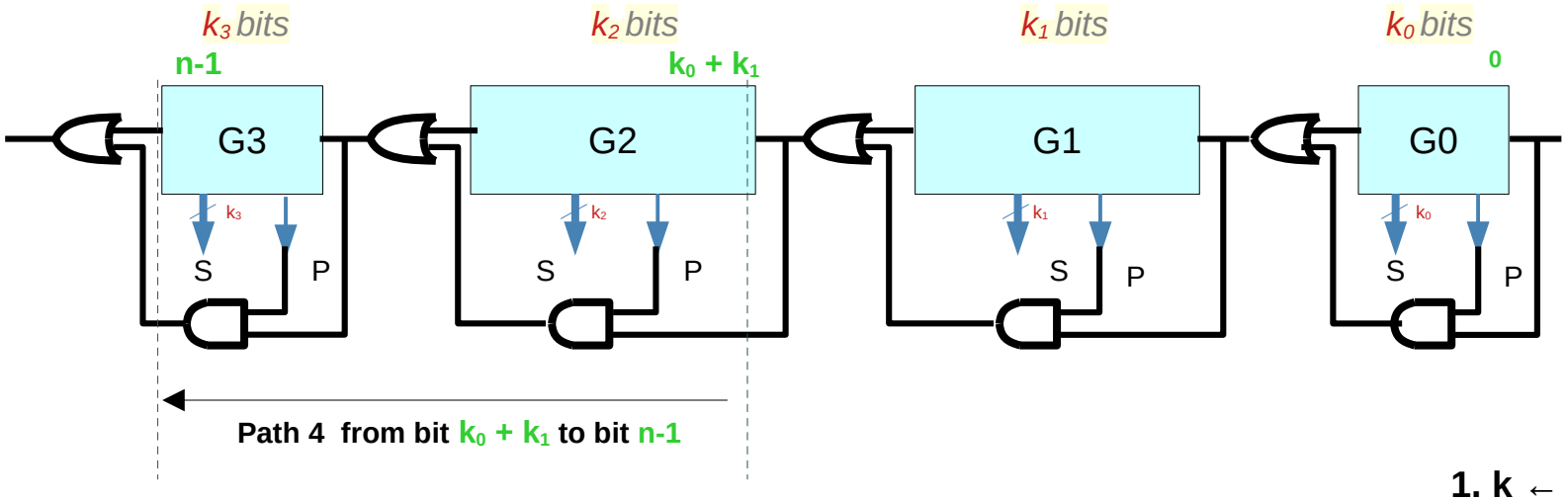
Similarly, if $k_2 = k_1 + 1$, the worst case delay
from stage ($k_0 + k_1$) to stage ($n - 1$)
will be no larger than the delay for path 1.

Blocks to the right of the center of the adder
may therefore have sizes
that form a simple incremental sequence.

Variable-size block CSA (VCSA)

R groups

$$n = \sum_{i=0}^{R-1} k_i$$



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1. **k ← n : total number of bits**
2. **b ← k : block size in bits**

Variable size Block Carry Skip Adder (9)

Variable-size block CSA (VCSA)

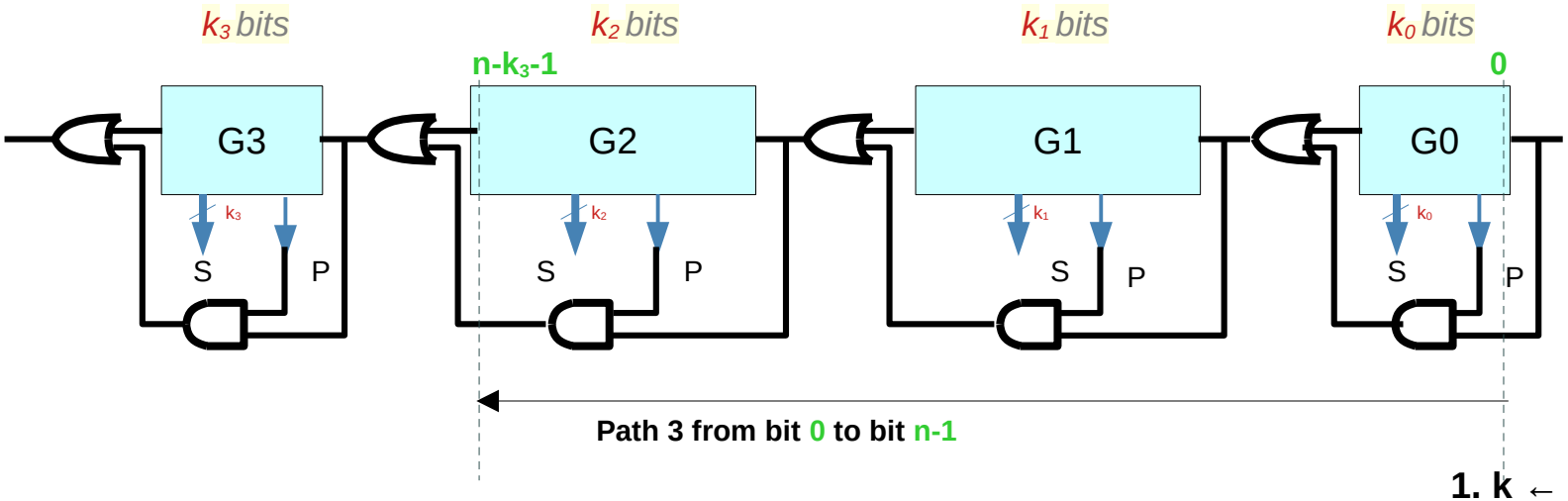
R groups

$$n = \sum_{i=0}^{R-1} k_i$$

Now consider a carry being generated in stage 0
and used (absorbed) in the left-most stage
of the penultimate (last but one; second last) block of the adder,
stage $n - k_{R-1} - 1$.

The delay of path 3

$$T_{path\ 3} = (k_{R-2} - 1)T_p + (R - 3)T_s + D + (k_0 - 1)T_p$$



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1. k ← n : total number of bits
2. b ← k : block size in bits

Variable size Block Carry Skip Adder (10)

Variable-size block CSA (VCSA)

R groups

$$n = \sum_{i=0}^{R-1} k_i$$

Compare this with the delay for path 1,
the longest carry-propagation path.

$T_{path\ 1} = (k_{R-1} - 1)T_p + (R - 2)T_s + D + (k_0 - 1)T_p$
$T_{path\ 3} = (k_{R-2} - 1)T_p + (R - 3)T_s + D + (k_0 - 1)T_p$

$T_{path\ 1} = T_{path\ 3}$ ➡ $(k_{R-1} - k_{R-2})\ T_p + T_s = 0$
$T_s = T_p$ ➡ $(k_{R-1} - k_{R-2}) + 1 = 0$

Again, if $T_p = T_s$, block size k_{R-2}
can be 1 bit larger than block size k_{R-1}
without making this delay path worse than path 1.

$(k_{R-1} - k_{R-2})\ T_p + T_s = ((k_{R-1} - k_{R-2}) + 1)T_p = 0$

$k_{R-2} = k_{R-1} + 1$

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1. k ← n : total number of bits
2. b ← k : block size in bits

Variable size Block Carry Skip Adder (11)

Variable-size block CSA (VCSA)

Blocks to the left of the center of the adder
may also have sizes that form a simple incremental sequence.

This analysis suggests an organ-pipe structure for the block sizes,

k, k + 1, · · ·, k+R/2− 1, | k+R/2 − 1, · · ·, k + 1, k

R/2 blocks R/2 blocks

R groups

$$n = \sum_{i=0}^{R-1} k_i$$

2, 3, 4, 5, 5, 4, 3, 2

2, 2+1, 2+2, 2+3, 2+3, 2+2, 2+1, 2

k=2, R=8

R =8 R/2=4 0, 1, 2, 3

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1. k ← n : total number of bits
2. b ← k : block size in bits

Variable size Block Carry Skip Adder (12)

Variable-size block CSA (VCSA)

Consider a 28 bit adder with carry-skip block sizes 2,3,4,5,5,4,3,2.

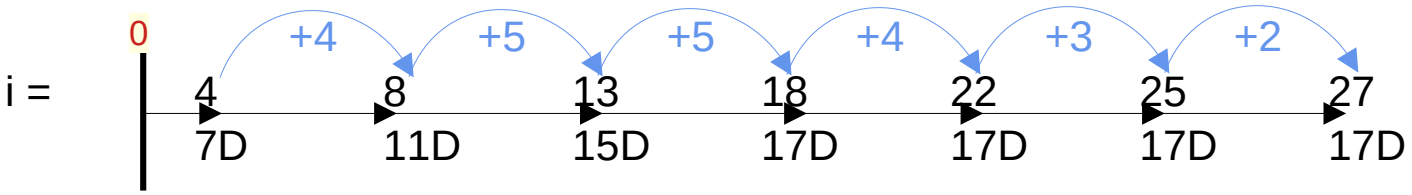
n = 28 = 2+3+4+5+5+4+3+2

R groups

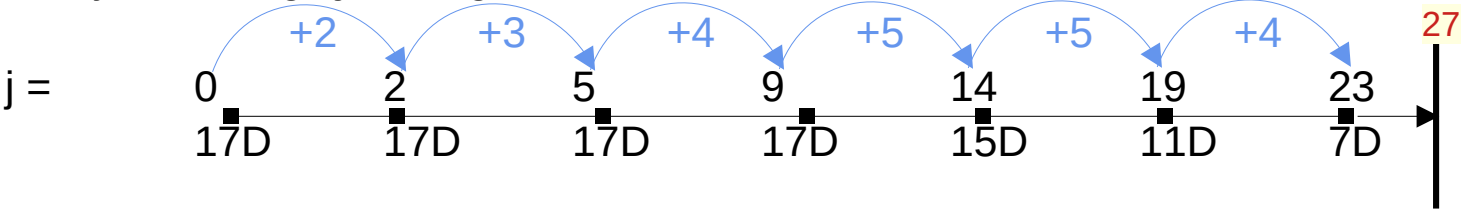
$$n = \sum_{i=0}^{R-1} k_i$$

The following tables show the worst case delay paths
for a carry generated in stage 0 and absorbed in stage i,
and for a carry generated in stage j and absorbed in stage 27.

Delay from stage 0 to stage ***i***



Delay from stage ***j*** to stage 27



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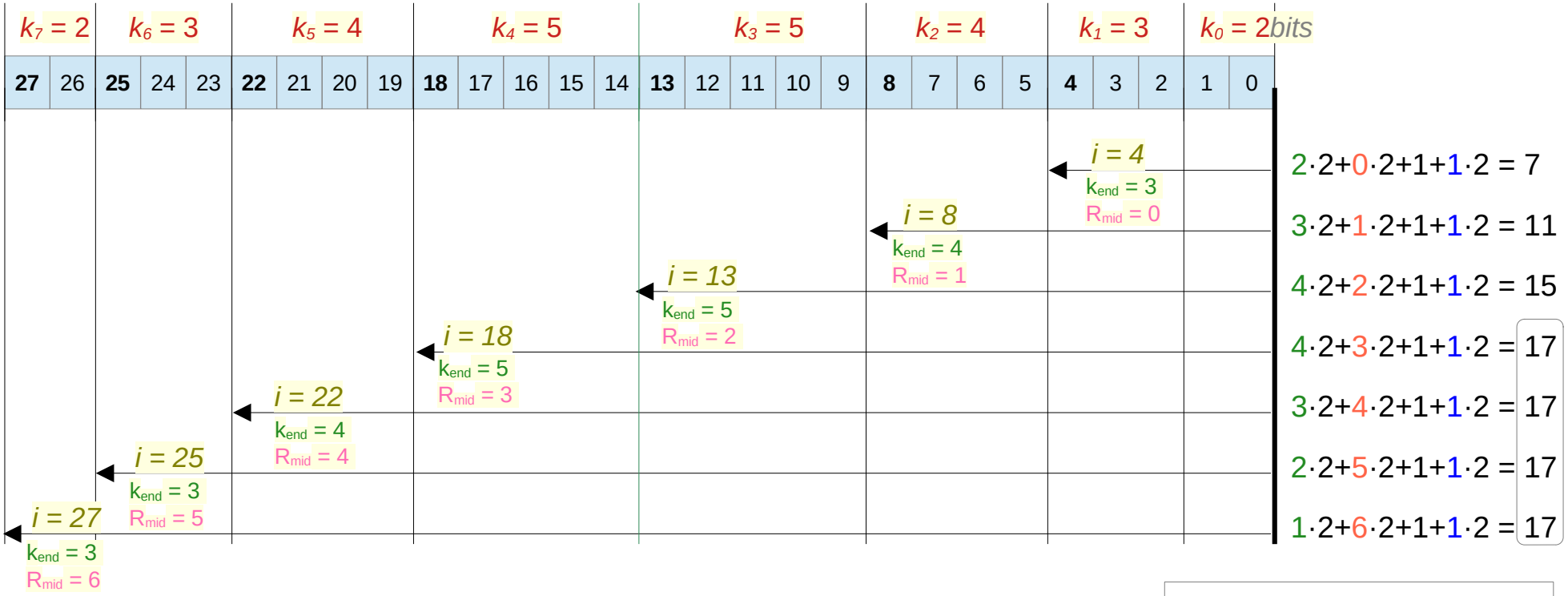
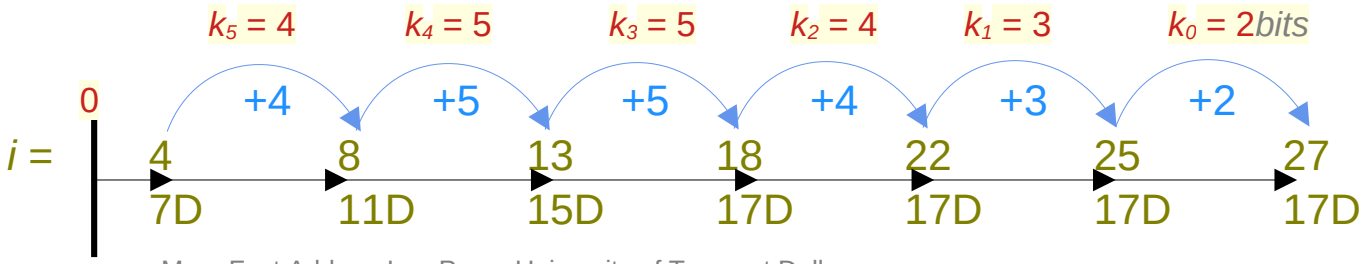
1. k ← n : total number of bits
2. b ← k : block size in bits

Variable size Block Carry Skip Adder (12)

$T_{path\ 1} = (k_{end} - 1)T_p + (R_{mid})T_s + D + (k_0 - 1)T_p$

n = 28, R= 8





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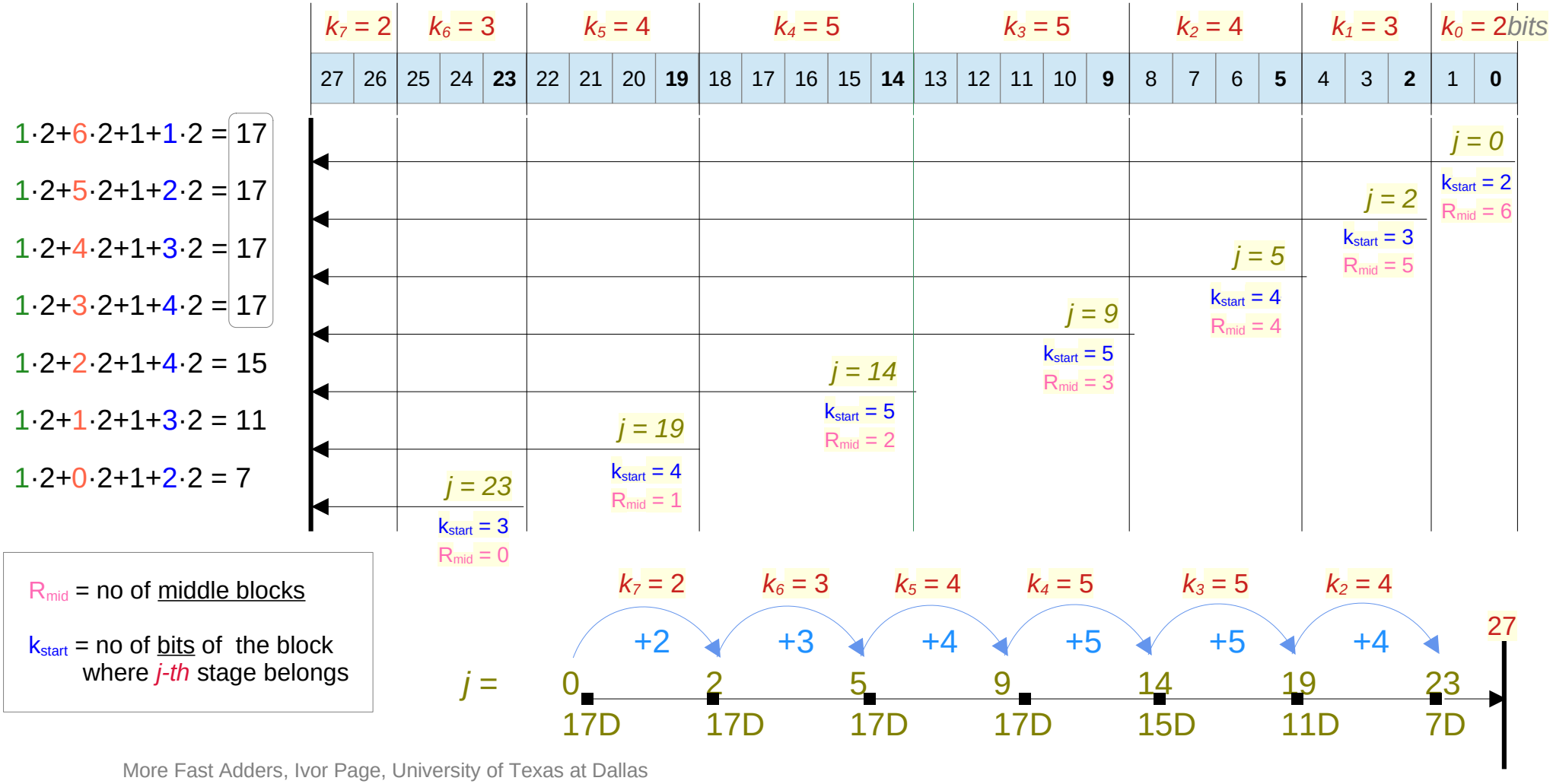
R_{mid} = no of middle blocks

k_{end} = no of bits of the block where *i-th* stage belongs

Variable size Block Carry Skip Adder (13)

$T_{path\ 3} = (k_{R-1} - 1)T_p + (R_{mid})T_s + D + (k_{start} - 1)T_p$

n = 28, R= 8



R_{mid} = no of middle blocks

k_{start} = no of bits of the block where *j-th* stage belongs

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Variable size Block Carry Skip Adder (13)

Variable-size block CSA (VCSA)

The worst case delays are

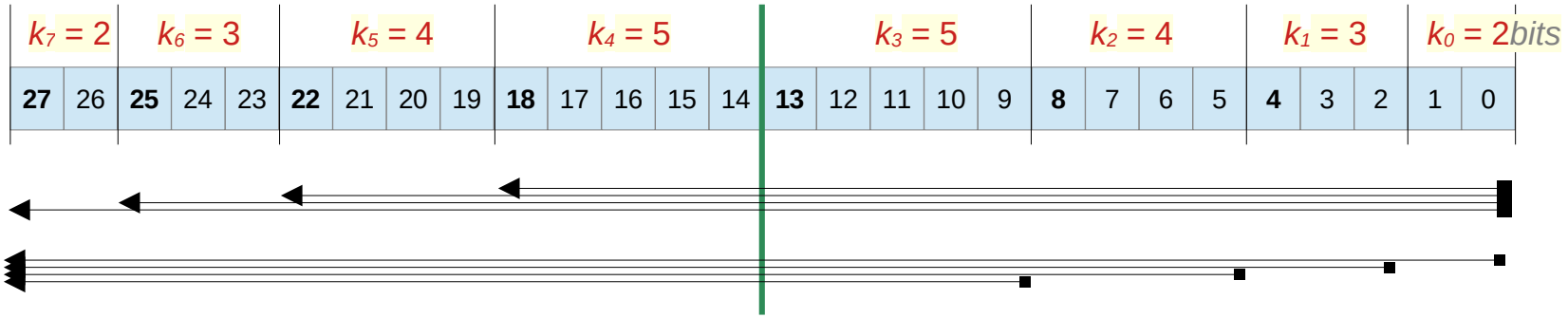
from carries generated in stage zero of the adder and absorbed anywhere in the left-hand half,

and from carries generated anywhere in the right-hand half and absorbed in stage 27.

These eight delays of 17D are made equal by making the block sizes vary in the organ-pipe fashion described above.

R groups

$$n = \sum_{i=0}^{R-1} k_i$$



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1. k ← n : total number of bits
2. b ← k : block size in bits

Variable size Block Carry Skip Adder (14)

Variable-size block CSA (VCSA)

The total number of bits in the R blocks is then:

$$2[k + (k + 1) + \cdots + (k + R/2 - 1)] = R(k + R/4 - 1/2) = n$$

$$(a + l)/2$$

$$2\ (R/2)\ (k + k + R/2 - 1)/2 = (R/2)\ (2k + R/2 - 1) = R\ (k + R/4 - 1/2)$$

which gives:

$$(k + R/4 - 1/2) = n/R$$

$$k = n/R - R/4 + ½$$
$$= 28 / 8 - 8/4 + ½$$
$$= 4 - 2 + ½$$
$$= 2\ ½$$

R groups

$$n = \sum_{i=0}^{R-1} k_i$$

1. k ← n : total number of bits
2. b ← k : block size in bits

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Variable size Block Carry Skip Adder (15-1)

Variable-size block CSA (VCSA)

The worst-case delay through the adder with variable block sizes is then:

$T_{var} = (k-1)T_p + (R-2)T_s + D + (k-1)T_p$

last block middle blocks OR first block

$= 2kT_p - 2T_p + RT_s - 2T_s + D$

$= 4kD - 4D + 2RD - 4D + D$ ⟵ $k = n/R - R/4 + ½$

$= 4(n/R - R/4 + ½)D + 2RD - 7D$

$= 4nD/R - RD + 2D + 2RD - 7D$

$= 4nD/R + RD - 5D$

R groups

$$n = \sum_{i=0}^{R-1} k_i$$

1. k ← n : total number of bits
2. b ← k : block size in bits

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Variable size Block Carry Skip Adder (15-1)

Variable-size block CSA (VCSA)

$T_{var} = (k-1)T_p + (R-2)T_s + D + (k-1)T_p$
$= 4nD/R + RD - 5D$

R groups

$$n = \sum_{i=0}^{R-1} k_i$$

The optimal number of blocks is calculated as follows:

$d\,T_{var} / d\,R = -4nD/R^2 + D = 0 \qquad DR^2 = 4nD$

$R^{opt} = 2\sqrt{n}$

$T^{opt}_{var} = 4nD/(2\sqrt{n}) + 2D\sqrt{n} - 5D$
$= 4\,D\sqrt{n} - 5D$

which is approximately $1/\sqrt{2}$ times smaller than with fixed block size.

$T^{opt}_{fixed} = 4\sqrt{2}\,D\sqrt{n} - 7D$

$T^{opt}_{var} / T^{opt}_{fixed} = (4\,D\sqrt{n} - 5D) / (4\sqrt{2}\,D\sqrt{n} - 7D) = (4\,D\sqrt{n}) / (4\sqrt{2}\,D\sqrt{n}) = 1/\sqrt{2}$

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1. k ← n : total number of bits
2. b ← k : block size in bits

Variable size Block Carry Skip Adder (16)

$T^{opt}_{var} = 4D\sqrt{n} - 5D$

Variable-size block CSA (VCSA)

R groups

$$n = \sum_{i=0}^{R-1} k_i$$

Example:
Continuing with our 32 bit adder example of the previous section,

$R^{opt} = 2\sqrt{n} = 2\sqrt{32} = 11.3$

If we choose R = 10,
then k = n/R − R/4 + ½
= 32/10 − 10/4 + 1/2
= 3.2 – 2.5 + 0.5 = 1.2.

Say we choose k = 1.

1. k ← n : total number of bits
2. b ← k : block size in bits

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Variable size Block Carry Skip Adder (17)

k, k + 1, · · ·, k+R/2− 1, k+R/2 − 1, · · ·, k + 1, k
k = 1, R = 10

1, 2, 3, 4, 5, 5, 4, 3, 2, 1
n = 2(1+2+3+4+5) = 2x15 = 30

$T^{opt}_{var} = 4\,D\sqrt{n} - 5D = (4\sqrt{30} - 5)D = 16.9D = 17D$

The block sizes are then 1,2,3,4,5,5,4,3,2,1,
which only covers 30 bits.
Its delay is 17D.

Variable-size block CSA (VCSA)

R groups

$$n = \sum_{i=0}^{R-1} k_i$$

1. k ← n : total number of bits
2. b ← k : block size in bits

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Variable size Block Carry Skip Adder (17)

Variable-size block CSA (VCSA)

R groups

$$n = \sum_{i=0}^{R-1} k_i$$

The adder with block sizes 1,2,3,4,5,5,4,3,2,1 has delay
1, 2, 3, 4, 5, 6, 7, 8

0 × 2D + D + 8 × 2D + 0 × 2D = 17D.

The adder with block sizes 1,1,2,3,4,5,5,4,3,2,1,1 has delay
1, 2, 3, 4, 5, 6, 7, 8, 9, 10

1 × 2D + D + 10 × 2D + 1 × 2D = 25D.

The adder with block sizes 2,2,3,4,5,5,4,3,2,2 has delay
1, 2, 3, 4, 5, 6, 7 8,

1 × 2D + D + 8 × 2D + 1 × 2D = 21D.

The adder with block sizes 1,4,5,6,6,5,4,1 also has delay 21D.
1, 2, 3, 4, 5, 6,

1 × 2D + D + 6 × 2D + 1 × 2D = 19D.

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1. k ← n : total number of bits
2. b ← k : block size in bits

Variable size Block Carry Skip Adder (17)

1,1,2,3,4,5,5,4,3,2,1,1 $R_m = 10$, k = 1 2(1+2+3+4+5) + 2(1) = 30 + 2 = 32

1, 2, 3, 4, 5, 6, 7, 8, 9, 10

2,2,3,4,5,5,4,3,2,2 $R_m = 8$, k = 2 2(2+3+4+5) + 2(2) = 28 + 4 = 32

1, 2, 3, 4, 5, 6, 7 8,

1,4,5,6,6,5,4,1 $R_m = 6$, k = 4 2(4+5+6) + 2(1) = 30 + 2 = 32

1, 2, 3, 4, 5, 6,

Variable-size block CSA (VCSA)

R groups

$$n = \sum_{i=0}^{R-1} k_i$$

$T_{var} = (k-1)T_p + D + (R-2)T_s + (k-1)T_p$ $R_m = R - 2$

$1 \times 2D + D + 10 \times 2D + 1 \times 2D = 25D.$

$1 \times 2D + D + 8 \times 2D + 1 \times 2D = 21D.$

$1 \times 2D + D + 6 \times 2D + 1 \times 2D = 19D.$

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1. k ← n : total number of bits
2. b ← k : block size in bits

Variable size Block Carry Skip Adder (18)

Notice here that the worst case delay
corresponds to a delay path
from the right-most stage of the right block of 6
to the left-most stage of the left block of 6.

As we discovered in the analysis,
there is a balance between the largest (or smallest) block size
and the number of blocks.

Compare these results with 35D obtained with fixed block sizes
and 128D obtained with a ripple-carry adder.

Our analysis gives optimal delay of 17.6D,
but we were only able to achieve 21D.

Variable-size block CSA (VCSA)

R groups

$$n = \sum_{i=0}^{R-1} k_i$$

1. k ← n : total number of bits
2. b ← k : block size in bits

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Variable size Block Carry Skip Adder (19)

Variable-size block CSA (VCSA)

For a 64 bit adder, the best sequence of block sizes appears to be:
2,4,5,6,7,8,8,7,6,5,4,2

and it has delay 29D
which is close to the optimum of 27D
for this type of adder.

Compare with 35D for the fixed block size adder
and 128D for the ripple-carry adder.

R groups

$$n = \sum_{i=0}^{R-1} k_i$$

1. k ← n : total number of bits
2. b ← k : block size in bits

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Variable size Block Carry Skip Adder (19)

Variable-size block CSA (VCSA)

For a 64 bit adder, the best sequence of block sizes appears to be:
2,4,5,6,7,8,8,7,6,5,4,2

1,2,3,4,5,6,7	7x(8) =56	(64-56)/2=4	2,1,2,3,4,5,6,7,7,6,5,4,3,2,1,2
2,3,4,5,6,7	6x(9) =54	(64-54)/2=6	3,1,2,3,4,5,6,7,7,6,5,4,3,2,1,3
3,4,5,6,7	5x(10)=50	(64-50)/2=14	7,3,4,5,6,7,7,6,5,4,3,7
4,5,6,7,8	5x(12)=60	(64-60)/2=4	2,4,5,6,7,8,8,7,6,5,4,2
5,6,7,8	4x(13)=52	(64-52)/2=6	6,5,6,7,8,8,7,6,5,6
6,7,8,9	4x(15)=60	(64-50)/2=2	2,5,6,7,8,8,7,6,5,2

R groups

$$n = \sum_{i=0}^{R-1} k_i$$

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1. k ← n : total number of bits
2. b ← k : block size in bits

Variable size Block Carry Skip Adder (20)

Further developments are possible with the carry-skip idea
if more than one level of skip units is employed.
We shall not study these developments.

The text has an example of a 30 bit adder
with two levels of carry-skip units and
a delay of 17D according to my calculations,
which is no better than the single layer scheme
for a 30 bit adder developed above.

Variable-size block CSA (VCSA)

R groups

$$n = \sum_{i=0}^{R-1} k_i$$

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1. k ← n : total number of bits
2. b ← k : block size in bits

References

[1] en.wikipedia.org
[2] Parhami, “Computer Arithmetic Algorithms and Hardware Designs”